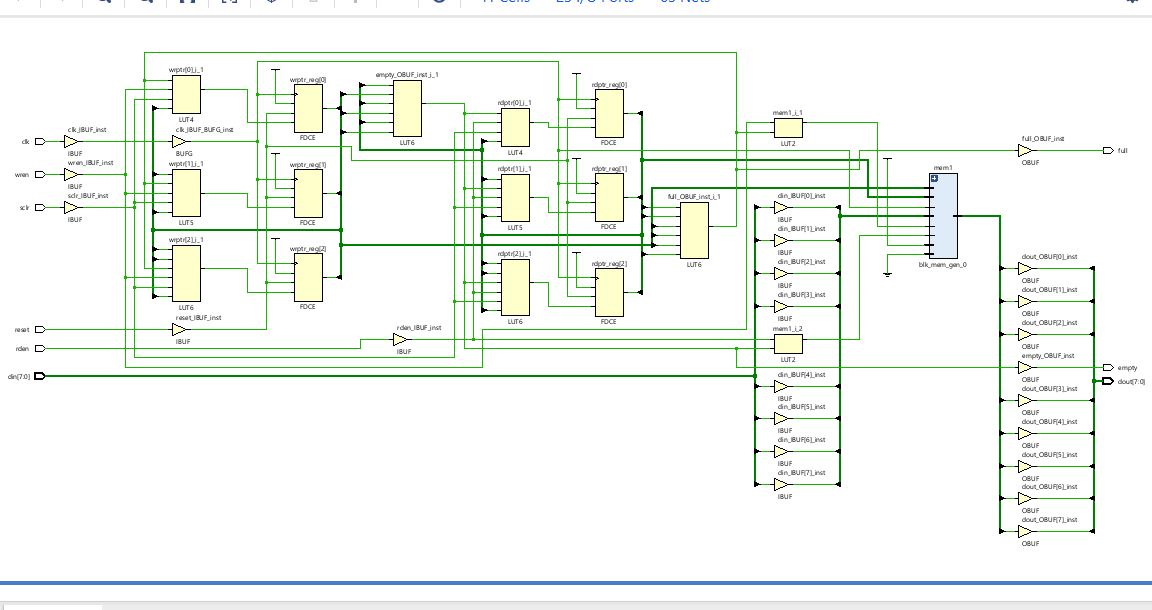
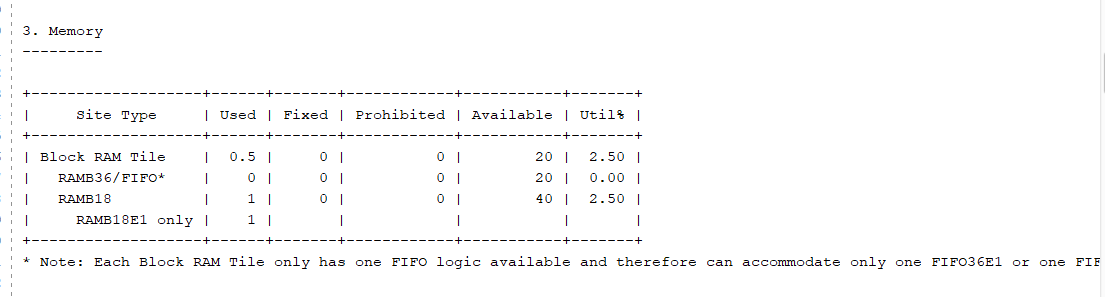
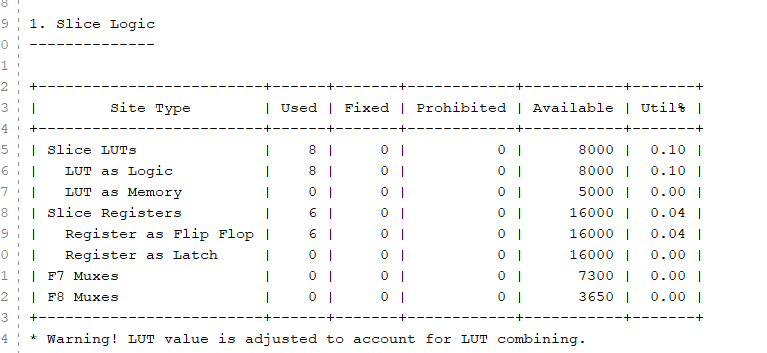
# Name: Cooper Medved

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1. Correct Design part 1 (90 pts)



1. Implementation tables – Slice Logic Table, Memory table (5 pts) – This is the first time your design has had Memory, so the Memory table will show that a block RAM tile is used.



1. Question (5 pts): For your design, assume the write counter value is "3", and the read counter value is "6". How many elements are in the FIFO?

FIFO # of elements = (Write counter – Read counter + Total capacity) which then (3-6+ 8) = 5 which means the number of elements is 5.